IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device having a field effect transistor, said field effect transistor comprising a semiconductor substrate, source and drain regions formed in said semiconductor substrate, a gate insulating film on said semiconductor substrate, and a gate electrode disposed via said gate insulating film on said semiconductor substrate,

said gate insulating film being an insulating film having a higher dielectric constant than that of a silicon dioxide film,

the upper end portions in the gate length direction of said gate insulating film being positioned inwardly from the respective end portions of the gate electrode and inwardly from respective lower end portions of said gate insulating film, on the source side and on the drain side of said gate electrode, and said upper end portions of said gate insulating film being positioned in a region in which said gate electrode overlaps with a the source region and athe drain region in plan configuration.

2. (Currently Amended) A semiconductor device having a field effect transistor, said field effect transistor comprising a semiconductor substrate, a gate insulating film on said semiconductor substrate, and a gate electrode disposed via said gate insulating film on said semiconductor substrate,

said gate insulating film being an insulating film having a higher dielectric constant than that of a silicon dioxide film, and the upper end portions in the gate length direction thereofof said gate insulating film being positioned inwardly from the

respective end portions of said gate electrodes and inwardly from respective lower end portions of said gate insulating film on the source side and on the drain side of said gate electrode, and

a source region and a drain region of said field effect transistor extending into the underlying portion of said gate insulating film.

3. (Original) The semiconductor device according to claim 1, wherein an insulating film having a lower dielectric constant than that of said gate insulating film is provided laterally of the end portions in the gate length direction of said gate insulating film, and on said semiconductor substrate.

4. (Currently Amended) The semiconductor device according to claim 1, wherein the upper end portions of the gate insulating film in the gate length direction of said gate insulating film are positioned inwardly from the respective end portions of the gate electrode on the source side and on the drain side of said gate electrode by 15 nm to 25 nm, respectively.

5. (Original) The semiconductor device according to claim 1, wherein said gate insulating film is an oxide, an oxynitride, or a silicate compound of at least one metal selected from the group consisting of titanium, tantalum, hafnium, zirconium, aluminum, lanthanum, and strontium.

6. (Withdrawn) The semiconductor device according to claim 1, wherein said gate insulating film has a laminated structure of a layer comprising an oxide of

at least one metal selected from the group consisting of titanium, tantalum, hafnium, zirconium, aluminum, lanthanum, and strontium, and

a layer comprising a silicate compound of said metal.

7. (Currently Amended) The semiconductor device according to claim 1, wherein said semiconductor substrate comprises a silicon substrate and wherein said source region and said drain region formed in said silicon substrate do not contain the metal contained in said insulating film, or contain said metal in a concentration of 10^{11} atom/cm^2 or less.

8. (Withdrawn) The semiconductor device according to claim 1, wherein said gate electrode is a metal selected from at least one selected from the group consisting of tungsten, titanium, and molybdenum, or a nitride thereof or a silicide thereof.

9. – 20. (Cancelled)

21. (New) A semiconductor device according to claim 1, wherein lower end portions of said gate insulating film are formed outwardly of the end portions of the gate electrode in said gate length direction.

22. (New) A semiconductor device according to claim 2, wherein lower end portions of said gate insulating film are formed outwardly of the end portions of the gate electrode in said gate length direction.

23. (New) A semiconductor device having a field effect transistor, said field effect transistor comprising a semiconductor substrate, source and drain regions formed in said semiconductor substrate, a gate insulating film on said semiconductor substrate, and a gate electrode disposed via said gate insulating film on said semiconductor substrate,

said gate insulating film being an insulating film having a higher dielectric constant than that of a silicon dioxide film,

wherein both said gate electrode and said gate insulating film overlap the source and drain regions in plan configuration,

wherein said semiconductor substrate is a silicon substrate, and

wherein said gate insulating film includes metal,

further comprising means for reducing an amount of metal introduced into said silicon substrate from said gate insulating film, said means including forming upper end portions in a gate length direction of the gate insulating film inwardly of end portions of the gate electrode and reducing the thickness of the gate insulating film beginning from said upper end portions of the gate insulating film in areas where said gate electrode extends over said source and drain regions.

24. (New) A semiconductor device according to claim 23, wherein said means for reducing the amount of metal introduced into said silicon substrate further includes reducing the thickness of the gate insulating film in a tapered manner between the upper end portions of the gate insulating film and lower end portions of said gate insulating film.

25. (New) A semiconductor device according to claim 24, wherein both said upper end portions and said lower end portions of said gate insulating film are formed in areas where the gate insulating film overlaps the source and drain regions.

26. (New) A semiconductor device according to claim 24, wherein said lower end portions are formed outwardly of the end portions of the gate electrode in the gate length direction.

27. (New) A semiconductor device according to claim 24, wherein the means for reducing the amount of metal introduced into the silicon substrate further comprises a second gate insulating film having a lower dielectric constant than said gate insulating film formed over areas of said gate insulating film underlying said gate electrode between said upper end portions and said lower end portions of said gate insulating film.

28. (New) A semiconductor device according to claim 27, wherein said second insulating film is comprised of silicon dioxide.

29. (New) A semiconductor device having a field effect transistor, said field effect transistor comprising a semiconductor substrate, source and drain regions formed in said semiconductor substrate, a gate insulating film on said semiconductor substrate, and a gate electrode disposed via said gate insulating film on said semiconductor substrate,

said gate insulating film being an insulating film having a higher dielectric constant than that of a silicon dioxide film,

wherein both said gate electrode and said gate insulating film overlap the source and drain regions in plan configuration,

wherein said semiconductor substrate is a silicon substrate, and

wherein said gate insulating film includes metal,

further comprising means for reducing an amount of metal introduced into said silicon substrate from said gate insulating film, said means including forming upper end portions of the gate insulating film inwardly in a gate length direction from end portions of the gate electrode, reducing the thickness of the gate insulating film in areas where the gate electrode extends over the source and drain regions by reducing the thickness of the gate insulating film in a tapered manner between the upper end portions of the gate insulating film and lower end portions of the gate insulating film, which lower end portions of the gate insulating film extend outwardly from the respective end portions of the gate electrode in said gate length direction,

wherein both said upper end portions and said lower end portions of said gate insulating film are formed in areas where the gate insulating film overlaps the source and drain regions, and

further comprising a second gate insulating film having a lower dielectric constant than said gate insulating film, the second gate insulating film being formed over areas of said gate insulating film under the gate electrode and between said upper end portions and said lower end portions of the gate insulating film.

30. (New) A semiconductor device according to claim 29, wherein said second insulating film is comprised of silicon dioxide.

31. (New) A semiconductor device according to claim 23, wherein the upper end portions of the gate insulating film in the gate length direction of said gate insulating film are positioned inwardly from the respective end portions of the gate electrode on the source side and on the drain side of said gate electrode by 15 nm to 25 nm, respectively.

32. (New) A semiconductor device according to claim 29, wherein the upper end portions of the gate insulating film in the gate length direction of said gate insulating film are positioned inwardly from the respective end portions of the gate electrode on the source side and on the drain side of said gate electrode by 15 nm to 25 nm, respectively.

33. (New) A semiconductor device having a field effect transistor, said field effect transistor comprising a semiconductor substrate, source and drain regions formed in said semiconductor substrate, a gate insulating film on said semiconductor substrate, and a gate electrode disposed via said gate insulating film on said semiconductor substrate,

said gate insulating film being an insulating film having a higher dielectric constant than that of a silicon dioxide film,

wherein said gate electrode and said insulating film overlap said source and drain regions in plan configuration, and

further comprising means for reducing fringe capacitance in said areas where said gate electrode overlaps said source and drain regions, said means including forming said gate insulating film so that upper end portions in the gate length direction of the gate insulating film are position inwardly of end portions of said gate

electrode and inwardly of lower end portions of said gate insulating film and said upper end portions of said gate insulating film are formed in a region in which the gate electrode overlap the source and drain regions in plan configuration.

34. (New) A semiconductor device according to claim 33, wherein said lower end portions in the gate length direction of said gate insulating film are formed outwardly of said end portions of said gate electrode and wherein said means for reducing fringe capacitance further comprises forming a second gate insulating film having a lower dielectric constant than said gate insulating film in an area covering the gate insulating film under the gate electrodes and between the upper end portions and lower end portions of the gate insulating film.

35. (New) A semiconductor device according to claim 33, wherein the upper end portions of the gate insulating film in the gate length direction of said gate insulating film are positioned inwardly from the respective end portions of the gate electrode on the source side and on the drain side of said gate electrode by 15 nm to 25 nm, respectively.